

Om Patel

ompatel.ca | omprakash.patel@mail.utoronto.ca | linkedin.com/in/om-patel-op

Experience

Quality & Automation Engineer Intern, Relay Financial – Toronto, ON May 2026 – Present

- Increased test coverage from 0% to 51.2% for core in-house payments service by leading integration-test development, building its CI/CD test pipeline, workers, coverage reporting, and service mocks for AWS and third-party dependencies
- Built company-wide Cursor Cloud Agent automation to generate integration tests from PR diffs, provisioning Dockerized test environments and cloud VMs to accelerate test creation and standardize coverage across engineering teams
- Expanded core banking automation to 265+ maintained tests by adding 45+ API, UI and Lambda workflows, while cutting Playwright runtime 42% through GitHub Actions parallelization and replacing flaky setup patterns with deterministic fixtures

Analyst Software Tester Intern, FNZ – Toronto, ON May 2025 – Aug 2025

- Reduced pending retest backlog by 50%+ and unblocked team specific development by identifying 30+ platform bugs and validating 75+ fixes across staging and user-test environments using SQL, RabbitMQ, API logs, and Postman
- Improved automated regression accuracy by 18% by debugging 45+ Cypress tests and converting manual Client Onboarding coverage into an end-to-end suite spanning 10+ workflows, edge cases, and core platform functionality
- Authored 6+ technical design documents for the FNZ-BMO Fund Classification workflow, translating Bloomberg and Morningstar data into client-facing dashboards, collateral calculations and downstream processing

Data Analyst & Administrative Assistant, University of Toronto – Toronto, ON May 2024 – Aug 2024

- Presented PEY Co-op insights and concrete improvement steps to 15+ staff by analyzing 1,200+ survey responses with regards to student interests, industry preferences and service quality in Excel
- Produced Annual and Seasonal Recruitment Reports by analyzing 2,000+ Excel student records to identify hiring trends

Projects

FPGA Sobel Vision Accelerator [Github](#) | Apr 2025

- Engineered a CPU-free FPGA vision accelerator on Arty A7-100T in SystemVerilog, integrating grayscale conversion and 3x3 Sobel edge detection, achieving 81,380 frames/s and 5.74x OpenCV throughput with 32 parallel lanes at 200 MHz
- Implemented custom Ethernet/UDP stack in RTL with MDIO/MII, ARP, IPv4, CRC/FCS and asynchronous FIFOs, streaming QVGA frames directly from FPGA to Streamlit dashboard at 30 FPS across 9,000 frames with zero transport errors

WearAlert [Github](#) | Apr 2025

- Co-engineered a wireless fall-detection system for real-time caregiver alerts, fusing BNO055 motion and DPS310 barometric data across ESP32, ESP8266, and STM32 to achieve <100 ms end-to-end latency at 9–10 Hz
- Developed STM32 hardware interfaces and firmware in C, integrating interrupt-driven UART, 400 kHz I2C, GPIO/EXTI, and timer-triggered DAC/DMA to receive sensor telemetry and control OLED feedback and real-time audio alerts

Bread Crumb Trail | MakeUofT 2026 HW Hackathon Winner [DevPost](#) | Feb 2026

- Engineered a navigation and SOS system on Arduino UNO Q (AppLab), integrating GNSS/GPS (I2C), SSD1306 OLED (I2C), and a GSM/LTE cellular module (UART) to provide live coordinates and breadcrumbs to Streamlit dashboard
- Implemented cloud integrations: Twilio API for SOS SMS (compressed trail summary), Google Maps API for route/waypoint visualization, and Gemini API for interactive emergency guidance and breadcrumb-based path prediction
- Awarded the Qualcomm Sponsor Prize, Best Use of Arduino UNO Q (out of 260+ submissions)

Radio Power Amplifier and Low-Pass Filter PCB [Github](#) | Jan 2025 - May 2025

- Constructed a Class E power amplifier and 7-stage maximally flat low-pass filter, obtaining 2.7W output power across antenna load (30dB gain) and 1.69% total harmonic distortion, meeting requirements for radio integration
- Designed a 2-layer PCB in Altium Designer for 16MHz and 60V operation, achieving 76% power efficiency
- Executed automated hardware unit testing using Python to interface with oscilloscope, DMM, and waveform generator

Skills

Languages: C, C++, Python, SystemVerilog, Verilog, RV32 Assembly, JavaScript, SQL

Design & Development: Vivado, Quartus, ModelSim, Altium, LTspice, MATLAB, SUE SoC, MMI MAX

Hardware: Arty A7-100T (Artix-7), DE1-SoC, STM32 (Cortex-M4), ESP32, Arduino, OV7670, Oscilloscopes, Soldering

Education

University of Toronto – BAsC in Electrical Engineering

Expected May 2028